REMARKS

Claims 1-4, 6, 14-17, 20 and 28-33 have been allowed.[1] Claims 21, and 25-27 stand rejected under 35 U.S.C. 102(b). Claims 5, 18-19 were cancelled in Applicants' previously-filed response.[2] Claims 7-13 and 22-24 stand objected to. Claims 1-4, 6-17 and 20-33 remain pending. The Examiner's claim rejections and objections are addressed below. Reconsideration of the application is respectfully requested.

Rejections Under 35 U.S.C. 102(b)

The Examiner rejected claims 21 and 25-27 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,698,869 to Yoshimi et al.[3] The Examiner's rejection is based on a disagreement over what it is that Yoshimi et al. actually discloses. Although that disagreement has persisted from some months now, Applicants believe that the argument presented below and the two documents attached hereto will pursuade the Examiner that Yoshimi et al. does not anticipate claims 21 and 25-27.

The Examiner is encouraged to refer now to the attached copy of FIG. 7 from the Yoshimi et al. reference. To facilitate the following discussion, certain features of FIG. 7 are provided with additional clarifying or new element labels. In this regard, the group of dislocation regions crossing the junction interface 215 is labeled "LEFT DISLOCATIONS". The other group of dislocation regions is labeled "RIGHT DISLOCATIONS". The junction proximate the RIGHT DISLOCATIONS is labeled "OTHER JUNCTION". The drain region 206 is additionally labeled "DRAIN REGION" and the source region 206 is additionally labeled "SOURCE REGION". The Examiner has taken the position that the junction interface 215 and the OTHER JUNCTION are actually are a singular junction.[4] Based on this assumption, the Examiner has opined that one of the

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[1]Appreciation is expressed for the allowance of claims 1-4, 6, 14-17, 20 and 28-33.

[2]Response to the Office Action Mailed September 25, 2003, filed on October 9, 2003.

[3]The element numbering used in Yoshimi et al. is followed herein.

[4]Office Action Mailed March 4, 2004, p. 4, paragraph 11.

LEFT DISLOCATIONS and one of the RIGHT DISLOCATIONS are not parallel in space and traverse what the Examiner believes is a singular junction. Applicants submit that the Examiner has misunderstood the structure disclosed in FIG. 7 and that such misunderstanding is likely based upon some unfortunate element numbering by the patentees in Yoshimi et al.[5] For example, the patentees improperly assigned the same element number 206 to both the n+ DRAIN REGION and the n+ SOURCE REGION, and the same element number 207 to both the silicon-germanium region in the n+ DRAIN REGION and the silicon-germanium region in the n+ SOURCE REGION. The Examiner has apparently assumed that the patentees continued this pattern of sloppy element numbering when assigning the number 215 to the junction proximate the LEFT DISCLOCATIONS, i.e., that the number 215 was intended to also apply to the OTHER JUNCTION. This assumption overlooks what the patentees described about FIG. 7. There is no question that the patentees identified and discussed the junction interface 215 and its relation to the DRAIN REGION 206. On col. 4, ll. 30-33, the patentees stated that "[t]he crystal defect region D was generated so as to traverse the pn junction interface 215 over the drain region 206 and the channel region 203." Significantly though, the patentees later individually discussed the junction between the SOURCE REGION and the channel region. On col., 4, ll. 47-52, the patentees stated that "in order to suppress effectively the floating body effect in the SOLMOSFET, the SiGe layer must be formed sufficiently close to the pn junction interface formed between the source region and the channel region . . . ." This is an unmistakable reference to another junction, namely the OTHER JUNCTION. If the Examiner's assumption were correct that element number 215 was intended to refer to both the junction 215 and the OTHER JUNCTION, one would have expected the patentees to have inserted the number 215 between the words "interface" and "formed" in the just quoted passage. But of course, they did not.

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[5]The causes for such element numbering are unknown, but may be due to the vagaries associated with melding six different prior Japanese patent applications into, and the subsequent translation into English of, a single gargantuan application and/or perhaps some sloppy drafting on the part of the attorneys representing the Yoshimi et al. inventor group.

Applicants believe that a three-dimensional depiction of a typical MOSFET will aid the Examiner's understanding. In this regard, Applicants have submitted herewith copies of pages 298-299 from Stanley Wolfe and Richard Tauber, Silicon Processing in the VLSI Era, Vol. 2.[6] The Examiner is respectfully directed to FIG. 5-1a on page 299, which provides an excellent three-dimensional representation of a MOSFET device. For the benefit of the Examiner, one of the pn junctions of the MOSFET in FIG. 5-1a has been designated JUNCTION 1 and the other of the pn junctions has been designated JUNCTION 2. The Examiner can appreciate that the two junctions, JUNCTION 1 and JUNCTION 2, do not in fact meet in space in that they are separated across the channel.[7]

Claim 21 recites, *inter alia*, a circuit device comprising first and second dislocation regions in a device region wherein the first and second dislocation regions are in non-parallel spatial relationship and traverse a junction. The Examiner is directed to the non-parallel dislocation regions 60 and 64 in FIG. 2 of Applicants' drawings. In contrast, the LEFT DISLOCATIONS is FIG. 7 of Yoshimi et al. are parallel in space and cross the junction 215. The RIGHT DISLOCATIONS are parallel in space and cross the OTHER JUNCTION. However two non-parallel dislocations do not cross a given junction, either 215 or the OTHER JUNCTION.

Applicants submit that claims 22-24 are patentable for the reasons advanced above for claim 21.

Applicants have amended claim 7 as suggested by the Examiner. The objection to that claim and claims 8-13 have been overcome.

Conclusion

For the extensive reasons advanced above, Applicants submit that claims 7-13, 21-27 are patentable and respectfully request that a Notice of Allowability issue in due course for those and the previously allowed claims.

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[6]This material is being submitted concurrently via a Supplemental Information Disclosure Statement.

[7]It is likely that a MOSFET device in which the source and drain share a singular pn junction would simply produce a short circuit between the drain and the source.

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Miscellaneous

The Assistant Commissioner is authorized to charge any required fees or credit any overpayment to Deposit Account No. 01-0365, Order No. AMDI:115\HON.

Respectfully submitted,

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